REMARKS

The Applicant thanks the Examiner for the careful examination of this application and respectfully requests the entry of the amendments indicated hereinabove.

Claims 1-29 are pending and rejected. Claims 6-7, 12-13, and 18-19 are amended hereinabove. In response to the drawing objections, FIGURES 1-2 have been amended plus FIGURE 4 has been added.

The Applicant is confused by the 35 U.S.C. §112, second paragraph rejections. Specifically, the well voltage is shown in both FIGURES 2 and 4. In addition, the substrate voltage is shown in FIGURE 4. The Applicant notes that the device claimed in Claims 11 and 23 are shown in FIGURE 4.

Independent Claim 1 positively recites a sleep mode voltage controller configured to provide both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode. These advantageously claimed features are not taught or suggested by the patent granted to Andersen et al.

Andersen et al. teaches away from the advantageously claimed invention because Andersen et al. teaches that the high voltage is allowed to float to a lower level (column 6 lines 5-9 and 44-54, column 7 lines 26-32 and 55-67, column 8 lines 1-4 and 42-46) and does not teach a controller that provides an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode as advantageously claimed (FIG. 11A). The Applicant respectfully traverses the assertion in the Office Action (page 4) that in FIG. 8 Andersen et al. discloses "a low-level power supply voltage of 0.3V higher than ground supply voltage during a sleep mode". The Applicant submits that Andersen et al. discloses keeping the low power supply voltage constant at zero volts (FIG. 11A). The "high level internal power supply voltage" and the "low-level power supply voltage" shown in FIG. 8 of Andersen et al. are the bounds within which the high cell voltage (i.e. the internal V_{dd}) is to be maintained by the power management circuit (column 7 line 39 through column 8 line 4).

Due to the foregoing reasons, the Applicant respectfully traverses the Examiner's rejection of Claim 1 and respectfully asserts that Claim 1 is patentable over Andersen et al. Furthermore, Claims 2-13 are allowable for depending on allowable independent Claim 1 and, in combination, including limitations not taught or described in the reference of record.

Independent Claim 14 positively recites providing both an array high supply voltage V_{ADD} that is lower than a high operating voltage V_{DD} and an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode. These advantageously claimed features are not taught or suggested by the patent granted to Andersen et al.

Andersen et al. teaches away from the advantageously claimed invention because Andersen et al. teaches that the high voltage is allowed to float to a lower level (column 6 lines 5-9 and 44-54, column 7 lines 26-32 and 55-67, column 8 lines 1-4 and 42-46) and does not teach providing an array low supply voltage V_{ASS} that is higher than a low operating voltage V_{SS} to the SRAM array during a sleep mode as advantageously claimed (FIG. 11A). The Applicant respectfully traverses the assertion in the Office Action (page 4) that in FIG. 8 Andersen et al. discloses "a low-level power supply voltage of 0.3V higher than ground supply voltage during a sleep mode". The Applicant submits that Andersen et al. discloses keeping the low power supply voltage constant at zero volts (FIG. 11A). The "high level internal power supply voltage" and the "low-level power supply voltage" shown in FIG. 8 of Andersen et al. are the bounds within which the high cell voltage (i.e. the internal V_{dd}) is to be maintained by the power management circuit (column 7 line 39 through column 8 line 4).

Due to the foregoing reasons, the Applicant respectfully traverses the Examiner's rejection of Claim 14 and respectfully asserts that Claim 14 is patentable over Andersen et al. Furthermore, Claims 15-23 are allowable for depending on allowable independent Claim 14 and, in combination, including limitations not taught or described in the reference of record.

Independent Claim 24 positively recites modifying the array high supply voltage V_{ADD} and the array low supply voltage V_{ASS} during transition from an active mode to the sleep mode. These advantageously claimed features are not taught or suggested by the patent granted to Andersen et al.

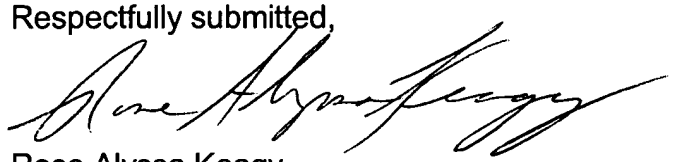
Andersen et al. teaches away from the advantageously claimed invention because Andersen et al. teaches disconnecting the major supply from the local supplies (column 6 lines 44-46, column 8 lines 42-46, column 2 lines 19-34) and does not teach modifying the array low supply voltage V_{ASS} during transition from an active mode to the sleep mode as advantageously claimed (FIG. 11A). The Applicant respectfully traverses the assertion in the Office Action (page 4) that in FIG. 8 Andersen et al. discloses "a low-level power supply voltage of 0.3V higher than ground supply voltage during a sleep mode". The Applicant submits that Andersen et al. discloses keeping the low power supply voltage constant at zero volts (FIG. 11A). The "high level internal power supply voltage" and the "low-level power supply voltage" shown in FIG. 8 of Andersen et al. are the bounds within

which the high cell voltage (i.e. the internal V_{dd}) is to be maintained by the power management circuit (column 7 line 39 through column 8 line 4).

Due to the foregoing reasons, the Applicant respectfully traverses the Examiner's rejection of Claim 24 and respectfully asserts that Claim 24 is patentable over Andersen et al. Furthermore, Claims 25-29 are allowable for depending on allowable independent Claim 24 and, in combination, including limitations not taught or described in the reference of record.

For the reasons stated above, this application is believed to be in condition for allowance. Reexamination and reconsideration is requested.

Respectfully submitted,



Rose Alyssa Keagy
Attorney for Applicant
Reg. No. 35,095

Texas Instruments Incorporated
PO BOX 655474, M/S 3999
Dallas, TX 75265
972/917-4167
FAX - 972/917-4409/4418

AMENDMENTS TO THE DRAWINGS:

The attached sheets of drawings include changes to FIGURES 1 and 2 (as indicated on the enclosed annotated sheets) and a new FIGURE 4. These sheets, which include FIGURES 1-4, replace the original sheets, which included FIGURES 1-3.

Attachments: Replacement Sheets

Annotated Sheet Showing Changes to FIGURES 1 and 2

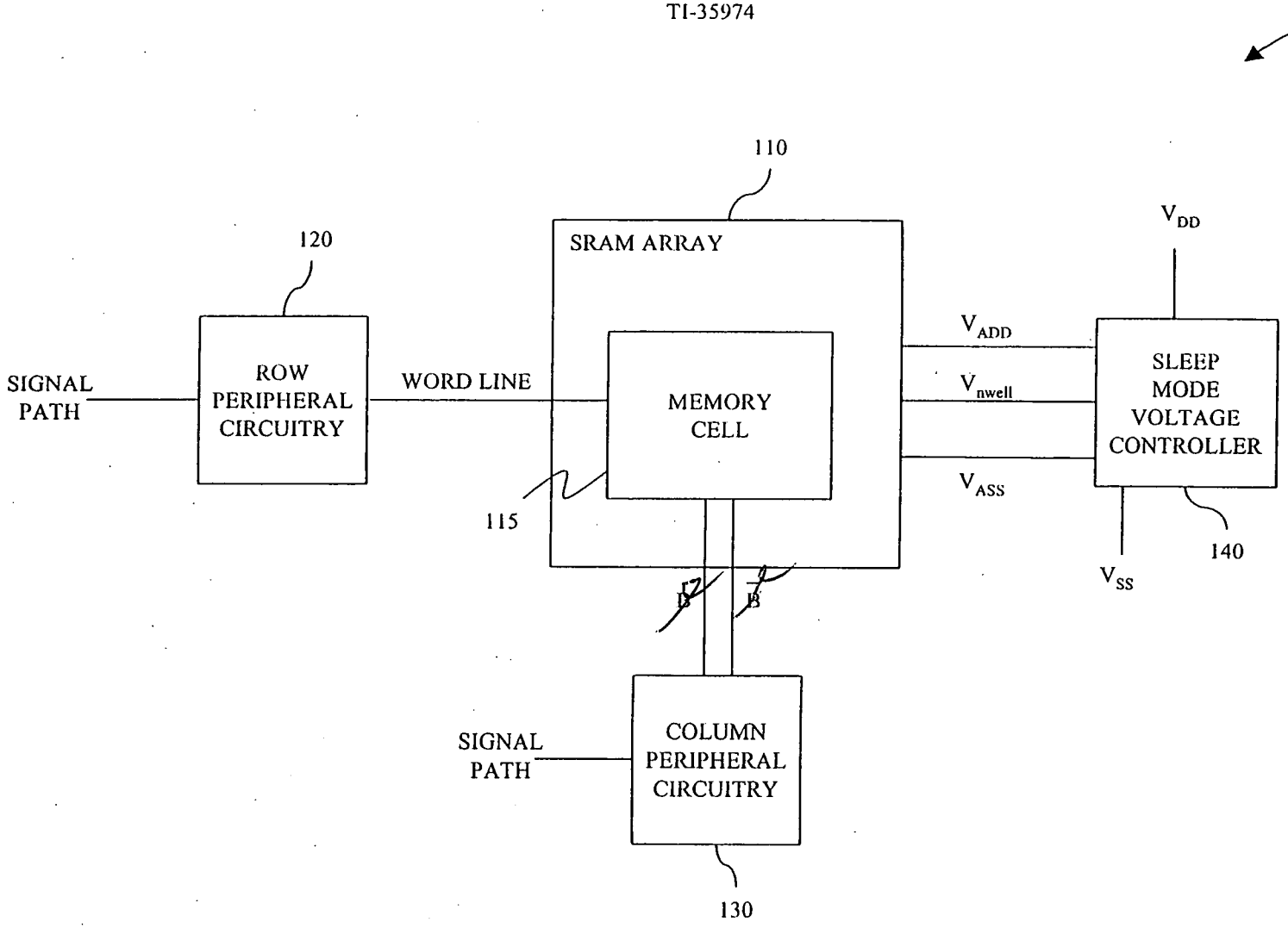


FIGURE 1

200

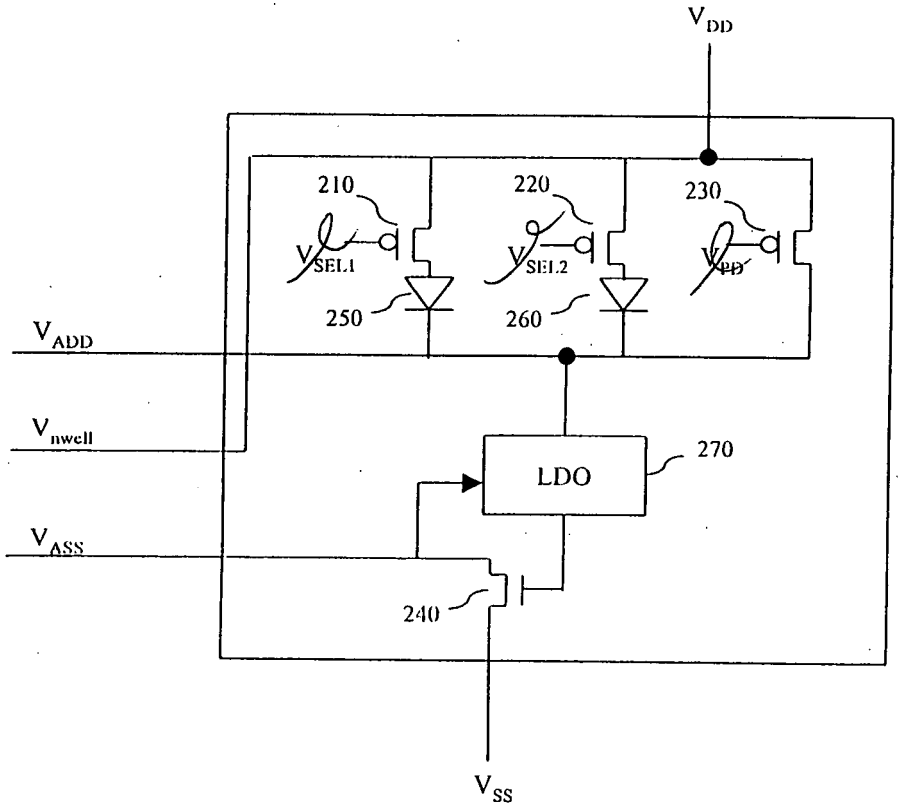


FIGURE 2